

CLAIMS:

What is claimed is:

- 1 1. A method for processing shadow register array control instructions, comprising:
- 2 fetching and decoding a shadow register array control instruction;
- 3 executing the shadow register array control instruction on data stored in a source
- 4 array of registers to write the data from the source array of registers to a destination array
- 5 of registers, the shadow array control instruction configured to provide a fast context save
- 6 during interrupt and non-interrupt processing.
- 1 2. The method according to claim 1, wherein the shadow register array control instruction
- 2 is a first shadow array control instruction.
- 1 3. The method according to claim 2, wherein the source array of registers is a primary
- 2 register array and the destination array of registers is a shadow register array.
- 1 4. The method according to claim 3, further comprising:
- 2 detecting that an interrupt condition has occurred.

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1 10. The method according to claim 9, wherein the second shadow register array control
2 instruction is executed before the execution of the return from the ISR routine.

1 11. A processor for performing shadow register array control instructions, comprising:
2 an array of primary registers for storing data;
3 an array of shadow registers for storing data;
4 a program memory for storing instructions including a shadow register array
5 control instruction;
6 a program counter for identifying current instructions for processing; and
7 a shadow register array control logic for executing the shadow register array control
8 instruction on a data stored in a source array of registers to write the data from the source
9 array of registers to a destination array of registers, the shadow register control instruction
10 configured to provide a fast context save during interrupt and non-interrupt processing.

1 12. The processor according to claim 11, wherein the shadow register array control
2 instruction is a first shadow array control instruction.

1 13. The processor according to claim 12, wherein the source array of registers is the array
2 of primary registers and the destination array of registers is the array of shadow
3 registers.

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1 14. The processor according to claim 12, further comprising:
2 interrupt logic for detecting that an interrupt condition has occurred.

1 15. The processor according to claim 14, further comprising:
2 an instruction register for loading the first shadow register array control instruction
3 for execution, the first shadow array instruction provided as a first instruction in an
4 interrupt service routine (ISR) for an interrupt servicing the interrupt condition.

1 16. The processor according to claim 11, wherein the shadow register array control
2 instruction is a second shadow array control instruction.

1 17. The processor according to claim 11, wherein the source array of registers is the array
2 of shadow registers and the destination array of registers is the array of primary
3 registers.

1 18. The processor according to claim 16, further comprising:
2 interrupt logic for detecting that an interrupt condition has occurred.

1 19. The processor according to claim 18, further comprising:
2 an execution unit for executing remaining instructions in an ISR for an interrupt
3 servicing the interrupt condition, the remaining instructions including a return from the

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4 ISR routine, wherein an automatic context save option in the return from the ISR routine is
5 disabled.

1 20. The processor according to claim 19, wherein the second shadow register array control
2 instruction is executed before the execution of the return from the ISR routine.

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